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A NOVEL REVERSIBLE DECODER FOR DESIGN AND SYNTHESIS OF COMBINATIONAL CIRCUITS

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Abstract: -

Reversible Logic has become one of the most promising research areas in recent decades and its applications in various technologies; As a CMOS with low consumption, nanotechnology and optical processing. The main purpose of designing reversible logic is to reduce quantum cost, depth of circuits, and number of waste products. The purpose of this document is to provide a framework, understanding, and review of reversible doors. In this document, various logical gates and their applicability to logical design are discussed. In addition, a brief overview of the comparison between reversible circuits based on various parameters is presented. The combination of decoders, comparators, full adders and multiplexers is designed using Fredkin Gate, CNT and GatePres, which offer better quantum costs than other reversible gates. Reversible logic circuits are designed and implemented using the VERILOG code, and the simulation results are obtained in Simulux ISE version 14.1.

Key words: CMOS, Fredkin Gate, CNT and GatePres, VERILOG code

I. INTRODUCTION

In current VLSI technology, power consumption has become an important consideration. Using a reversible decoder to design combination circuits reduces the power consumption optimally compared to conventional decoder based combination circuits. Reversible Logic finds its own application in quantum computing, nanotechnology, optical computing, computer graphics and low power VLSI. Ralph Launder [1] stated that the thermal dissipation of the circuits is not due to the process involved in the operation, but to the bits that were cleared during the process. He presented that the loss of a single bit in the circuit can be attributed to the smallest heat in the calculation, which is equivalent to 2 jt of KTLN, where K is the Boltzmann constant and T is the temperature. Although the amount of heat spread in simple circuits is small, it becomes larger in complex circuits, which also implies propagation delay. Later, in 1973, C. H. Bennett [2] explained that the power dissipation caused by the bit loss can be overcome if each of the calculations in the circuit is reversed. Quantum networks are designed by quantum logic gates. The KTln2 joules energy distribution will not occur if each gate has a unified operation, reversing the calculation. Therefore, there is no need to clear bits for reversible computations. The amount of heat spread over the system is directly related to the number of bits that are cleared or lost during the calculation.

II. CONCEPT

The use of reversible gates in reversible logic involves the same number of inputs and p outputs, that is, one to one mapping between input vectors and output output vectors. They can also run in the backward direction. There are some limitations to be considered when designing circuits based on reversible logic: (i) fan outing is not allowed in reversible logic; (ii) feedback is not allowed in reversible logic. In reversible logic using P outputs we can get complete knowledge about the inputs. Reversible logic saves information. Some measures, such as waste p outputs, number of gates, quantum cost, and fixed inputs, are used to measure the performance of reversible circuits. Waste p outputs are additional p outputs that help equalize inputs and p outputs to maintain reversibility. It leaves them alone with no activity. The number of gates is not a good metric, as more and more gates can form a new gate. Quantum cost is the number of primary or primitive gates required to implement the gate. This is just the number of reversible gates (1 × 1 or 2 × 2) needed to build the circuit. Delays are a major cost measure. Reversible circuit design can be modeled as a series of separate time slices, and depth is the summary of total time slices. In digital electronics, the binary decoder is a combination logic circuit that converts the binary integer value into the corresponding output output pattern. Various proposals have been devoted to the design of combination and sequential circuits in the ongoing research. In this paper, we suggest the design of different combination circuits, binary comparator, full adder, full subtractor, and multiplexer circuits using reversible decoder at excellent quantum cost.

III. REVERSIBLE LOGIC GATES

The basic Reversible Logic Gates present in the literature are briefed below. The gates that are suitable for the design with optimum quantum cost can be selected.

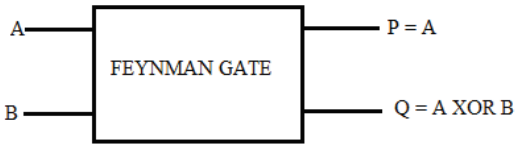
1. *NOT GATE:* Not Gate is simple Reversible logic gate. It is a 1 × 1 reversible logic gate with quantum cost zero. As shown in Figure 1, the gate gate converts the input complement to the output. This is the basic primitive gate that may be involved in the construction of the reversible logic gate Importance in determining the quantum cost of a designed reversible logic gate.

A	P
0	1
1	0

Fig. 1 NOT Gate and its Truth Table

2. *FEYNMAN GATE (FG):*

The Feynman Gate is a 2 × 2 reversible gate, as shown in Figure 2. Feynman Gate is also known as Sinot Gate, which means restricted note gate. Feynman Gate is used to duplicate the required p output as fan-out is not allowed in reversible logic gates. The quantum cost of FG is 1. It is also a primitive gate because of its importance in determining the quantum cost.

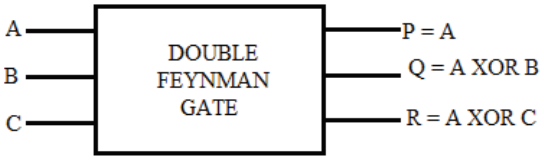


A	B	P	R
0	0	0	0
0	1	0	1
1	0	1	1
1	1	1	0

Fig. 2 Feynman Gate and its Truth Table

3. *DOUBLE FEYNMAN GATE (DFG):*

The double Feynman Gate is a 3 × 3 reversible gate. The p outputs are defined as shown in Figure 3 below. Quantum cost of DFG 2. This gate can also be used to duplicate p outputs.

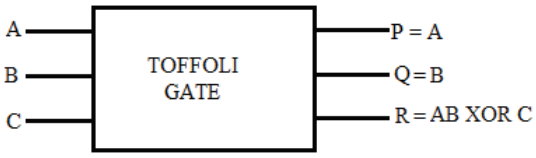


A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	1	1
1	0	1	1	1	0
1	1	0	1	0	1
1	1	1	1	0	0

Fig.3.Double Feynman Gate and its Truth Table

4. *TOFFOLI GATE*

(TG): Toffoli Gate is 3×3 reversible gate. The outputs are defined as shown in the below figure4. The Quantum Cost of TG is 4.

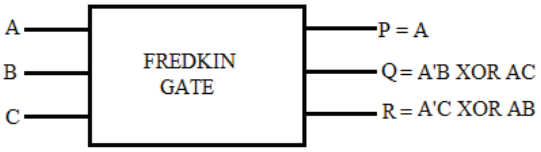


A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	1	0	1
1	1	0	1	1	1
1	1	1	1	1	0

Fig.4 Toffoli Gate and its Truth Table

5. *FREDKIN GATE (FDG):* Fredkin Gate is a 3×3

reversible gate. The outputs are defined as shown in the below figure4. The Quantum Cost of FDG is 5. This paper mainly surrounds around Fredkin gate.



A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	1	1	0
1	1	0	1	0	1
1	1	1	1	1	1

Fig.5 Fredkin Gate and its Truth Table

IV. BASIC GATES USING REVERSIBLE GATES

AND & OR gates should be designed with reversible gates according to our circuit requirements. We used the Fredkin gate to design the AND, or gates, as shown in Figure 6. Fredkin Gate is important because it is optimistic

AND, or quantum cost effective performance for designing gates..

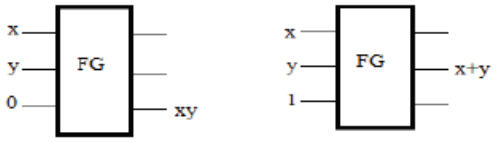


Fig.6 AND Gate using fredkin and OR Gate using fredkin

V.SIMULATION RESULTS

To design a multiplexer using reversible decoder, reversible 2 input AND gates, 2 input OR gates are required.The 2 input AND Gate and OR gate are designed
using Fredkin gate. By using these designed gates we can improve those gates to the required number of input gate. Each output line from decoder is driven to 2 input AND gate along with multiplexer input. The outputs of all AND gates are made to drive to that particular input OR gate. The input binary integer values act as the selection lines. Similarly by using 4×16 decoder a 16×1 multiplexer is designed. The RTL Schematic and the simulated outputs of 16×1 multiplexer are shown in figure.

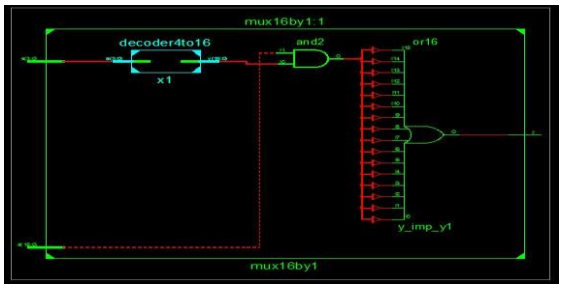


Fig.7. RTL Schematic of 16x1 multiplexer

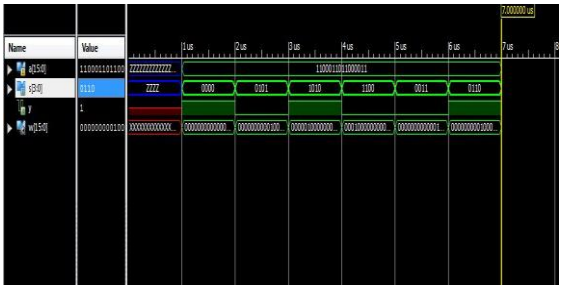


Fig.8.simulated output of 16x1 multiplexer

a.ADD – SUB:

To design 4-bit full adder/subtractor circuit four full adders are required. The Cin input drives the first full adder. If Cin is given with low input 4-bit addition is performed and if Cin is given with high input the 4-bit subtraction in the form of 1's complement addition is performed

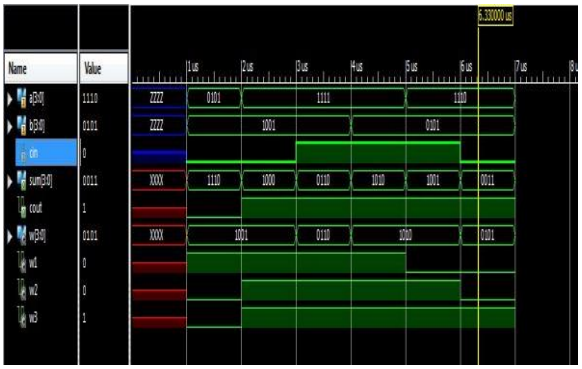


Fig.9. Simulated output of add-sub

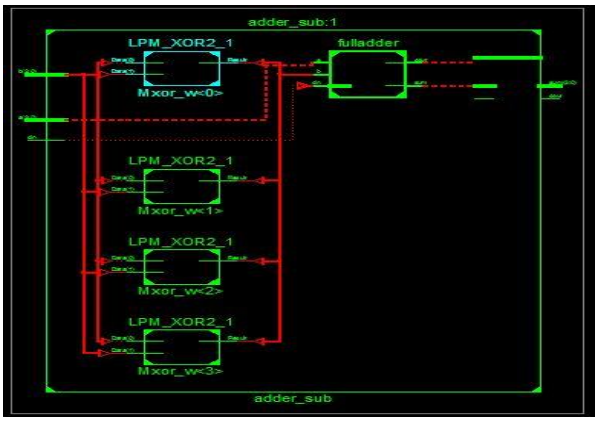


Fig.10. RTL Schematic of add-sub

b.5 TO 32 DECODER:

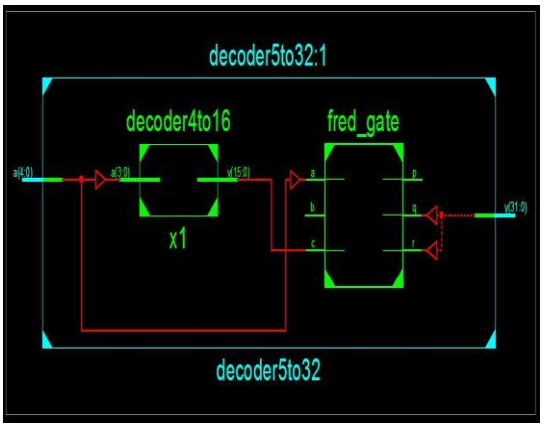


Fig.11. RTL Schematic of 5 to 32 decoder

Fig.12. Simulated output of 5 to 32 decoder

c.2 – BIT COMPARATOR:

The output lines g, l, e represents Greater, Lesser, Equal respectively. The a, b lines represents the inputs. If a<b then 'l' output becomes high. If a>b then 'g output ' becomes high.If a=b then output e becomes high.

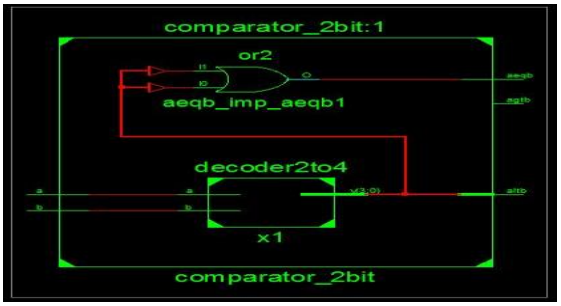


Fig.13. RTL Schematic of 2 – bit comparator

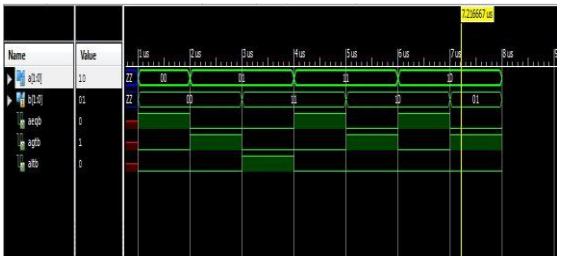


Fig.14. Simulated output of 2 bit comparator

VI. COMPARATIVE STUDY

The combinational circuits designed using reversible decoder are analyzed in terms of Quantum cost .

Parameter	Quantum Cost	
	Existing	Proposed
5 to 32 decoder	155	151
2 bit comparator	140	136
16x1 MUX	150	146
4-bit Adder/Subtractor	264	248

VII. CONCLUSION

In this paper, different combination circuits such as adder/subtractor,comparator, multiplexer, and decoder are compared. These circuits are designed for low quantum cost. The proposed method can be generalized to design the decoder circuit. The idea of duplicating the single output output to the output output required to overcome the fan-limit constraint in reversible logic circuits is used. This method of designing combination circuits enables many digital circuits to be implemented with great performance at minimum quantum cost.

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