Journal of Advanced Research in Technology and Management Sciences
Volume: 05 Issue: 06 ISSN: 2582-3078 June 2023
Available online at: http://www.jartms.org

Addressing Leakage Power in VLSI Design: Strategies, Trends, and Future

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Abstract- **Leakage power has emerged as a critical concern in VLSI design due to the relentless scaling of transistor dimensions and increasing transistor count on integrated circuits. As technology nodes continue to shrink, leakage power has become a dominant component of the overall power consumption, leading to performance degradation, reduced battery life, and increased heat dissipation. This review paper provides a comprehensive analysis of leakage power in VLSI design, focusing on its sources, challenges, and potential solutions. Various techniques for leakage power reduction at the circuit and architecture levels are discussed, including power gating, multi-threshold voltage techniques, supply voltage scaling, and process optimizations. Additionally, leakage power models and estimation methods are explored, along with trade-offs and design challenges associated with leakage power reduction. The paper also presents case studies and experimental results to illustrate the effectiveness of leakage power reduction techniques in practical designs. The insights provided in this review paper will aid researchers and practitioners in understanding the complexities of leakage power and making informed decisions during VLSI design to mitigate its adverse effects.**

Keywords **— VLSI design, leakage power, power gating, multi-threshold voltage, supply voltage scaling, process optimization, power consumption.**

I. INTRODUCTION

The continuous advancement of VLSI technology has enabled the integration of an ever-increasing number of transistors on a single chip. However, this scaling trend has also brought about significant challenges, one of which is the escalating issue of leakage power. Leakage power, which was once negligible, has become a dominant factor in overall power consumption, adversely impacting performance, battery life, and thermal management. This review paper aims to delve into the sources, consequences, and potential solutions for leakage power in VLSI design. By exploring various techniques and trade-offs, this paper provides valuable insights for addressing the critical issue of leakage power and achieving energy-efficient VLSI designs. The relentless pursuit of miniaturization and increased transistor density in VLSI design has led to significant advancements in the field of electronics. However, these advancements have come with their own set of challenges, one of the most critical being leakage power. Leakage power refers to the power consumed by a transistor when it is in an idle or off state, resulting from imperfections in the manufacturing process and subthreshold leakage currents. With each technology node shrink, the transistor dimensions have decreased, leading to an exponential increase in leakage current. As a consequence, leakage power has become a major contributor to the overall power dissipation in modern VLSI designs, rivaling the dynamic power consumed during active operations. This increased leakage power not only affects the performance and reliability of integrated circuits but also poses significant challenges in terms of thermal management and battery life, particularly in mobile and battery-operated devices. The objective of this review paper is to provide a comprehensive analysis of leakage power in VLSI design, focusing on its sources, challenges, and potential solutions. By understanding the various sources of leakage power, such as static power, sub threshold leakage, gate leakage, and reverse bias leakage, researchers and practitioners can devise effective strategies to mitigate its impact. Furthermore, this paper explores a range of leakage power reduction techniques, including power gating, multi-threshold voltage techniques, supply voltage scaling, and process optimizations. The discussion encompasses both circuit-level and architecture-level approaches, highlighting their advantages, limitations, and trade-offs. Additionally, this review paper presents an overview of leakage power models and estimation methods, which play a crucial role in accurately assessing and optimizing leakage power during the design phase. Practical case studies and experimental results are also discussed to illustrate the effectiveness of leakage power reduction techniques in real-world VLSI designs. By addressing the critical issue of leakage power, this review paper aims to facilitate the development of energy-efficient VLSI designs, enabling enhanced performance, longer battery life, and improved reliability in future electronic devices.

II. LEAKAGE POWER ANALYSIS AND MEASUREMENT TECHNIQUES

Accurate analysis and measurement of leakage power are essential for understanding and mitigating the impact of leakage power in VLSI designs. This section focuses on the various techniques employed to analyze and measure leakage power, enabling designers to gain insights into the

sources and magnitude of leakage power in their designs. Leakage Power Analysis Methodologies: Leakage power analysis methodologies involve the characterization of leakage currents at different design abstraction levels. Gate-level analysis techniques involve modeling leakage power based on transistor-level parameters such as threshold voltage, subthreshold leakage current, and gate leakage current. Circuit-level analysis techniques consider the impact of process variations, temperature, and supply voltage on leakage power. System-level analysis techniques examine the overall leakage power consumption in a VLSI system and enable power optimization at the architectural level. Experimental Characterization of Leakage Power: Experimental characterization of leakage power involves the measurement and analysis of leakage currents in real VLSI designs. Techniques such as source meter units, transistor-level simulations, and power sensors are commonly employed to measure leakage power. Specialized test structures, such as sleep transistors or low-leakage test circuits, are used to isolate and quantify leakage currents accurately. The industry has responded to market demands for efficient portable electronic devices by focusing on the development of circuit designs that operate at low voltage (LV) levels. This approach is aimed at achieving low power (LP) consumption, meeting the needs of consumers seeking energy-efficient products. The reduction in supply voltage results in a quadratic decrease in dynamic power and a linear decrease in leakage power to the first order [4]. and additionally, technologies such as silicon debug and power profiling tools provide valuable insights into leakage power during different operating modes and scenarios. Visualization Techniques: Diagrams and visualization techniques play a crucial role in understanding leakage power distribution and its impact on VLSI designs. Leakage power maps can be generated to identify regions of high leakage power density, enabling designers to target specific areas for leakage reduction. Histograms and statistical analysis can provide a comprehensive view of leakage power variations across different design corners, process variations, and environmental conditions. In summary, leakage power analysis and measurement techniques offer valuable tools for designers to assess and optimize leakage power in VLSI designs. By utilizing these techniques in combination with accurate modeling and simulation, designers can make informed decisions to reduce leakage power, improve energy efficiency, and enhance the overall performance of their VLSI designs.

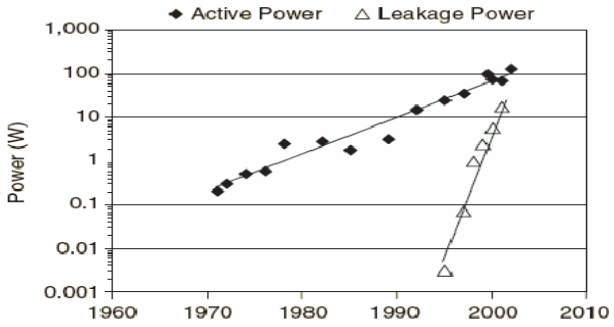

Fig.01: Active and leakage power dissipation [1]

III. EMERGING TRENDS AND FUTURE DIRECTIONS IN LEAKAGE POWER REDUCTION .

As the demand for energy-efficient VLSI designs continues to grow, researchers are exploring new approaches and technologies to tackle the challenges posed by leakage power. This section highlights some of the emerging trends and future directions in leakage power reduction, paving the way for more efficient and sustainable VLSI designs. Alternative Transistor Technologies: Researchers are investigating alternative transistor technologies that can effectively mitigate leakage power. This includes exploring options such as tunneling transistors, nanowire transistors, and steep slope devices that offer improved control over leakage currents and subthreshold leakage. Advanced Device Architectures: Novel device architectures are being developed to minimize leakage power. FinFETs, nanosheet FETs, and nanowire FETs are examples of advanced transistor structures that provide better control over leakage currents while maintaining high performance. Energy-Aware Design Methodologies: Design methodologies that prioritize energy efficiency are gaining traction. Techniques such as approximate computing, voltage overscaling, and near-threshold computing aim to strike a balance between performance and energy consumption, minimizing leakage power without significant performance degradation. The concept of intelligent power management involves understanding the device physics behind subthreshold and gate leakage, along with their correlation with circuit design variables [3]. Dynamic power management algorithms that adaptively optimize power based on workload characteristics, temperature, and performance requirements are being developed to reduce leakage power while ensuring optimal system operation.

Design	**Employed Strategy**
Level related to circuit or logic	Sizing of transistor and energy recovery

Level related to Architecture	Various encoding schemes ,pipelining strategies
Level related to Software	Strategy related to locality and concurrency
Level related to Technology	Reduction of threshold values, supporting multiple threshold distribution
Level related to Operating System	Dividing in portions and power down solution

Table.01: Strategies for low power design [2]

IV. SYSTEM-LEVEL POWER MANAGEMENT STRATEGIES FOR LEAKAGE POWER

To address the challenge of leakage power in VLSI designs, system-level power management strategies are crucial. These strategies aim to optimize power consumption by considering the entire system's operation and identifying opportunities for leakage power reduction. By adopting system-level approaches, designers can achieve substantial improvements in energy efficiency and mitigate the impact of leakage power. This section explores some key strategies employed at the system level for leakage power management. Dynamic Voltage and Frequency Scaling (DVFS): DVFS is a widely-used technique that adjusts the operating voltage and frequency of the system components based on workload demands. By dynamically scaling voltage and frequency, the system can operate at lower power modes during idle or low-demand periods, reducing leakage power without sacrificing performance. Adaptive Power Management Schemes: Adaptive power management schemes utilize real-time monitoring and analysis of system parameters to dynamically adjust power settings. These schemes consider workload variations, temperature conditions, and user requirements to optimize power consumption, effectively minimizing leakage power in different operational scenarios. Co-Design Methodologies: Co-design methodologies involve the joint optimization of hardware and software components to achieve power-efficient system operation. By considering both the hardware architecture and software algorithms, designers can identify power-hungry components and develop tailored power management techniques to target leakage power reduction. Power Gating and Sleep Modes: System-level power management includes the use of power gating techniques and sleep modes to selectively disable or reduce power to idle or unused components. By effectively powering down or reducing power to specific modules or subsystems, leakage power can be significantly reduced. These system-level power management strategies provide a holistic approach to mitigate leakage power in VLSI designs. By considering the system as a whole and adopting techniques such as DVFS, adaptive power management, co-design methodologies, and power gating, designers can achieve optimal energy efficiency and extend battery life in a wide range of electronic devices. Network communication is a group of nodes that are interconnected with telecommunication links, which are utilised for exchanging messages between nodes[5] . The importance of encrypting data is more pertinent in light of the mushrooming applications and globalization of communication[17] In a circuit three components are responsible for power dissipation: dynamic power, short-circuit power and static power. Out of these, dynamic power or switching power is primarily power dissipated when charging or discharging capacitors and is described below [6]. $P_{dyn}= C_L V_{dd} 2\alpha_f$-------- (i) Where C_L represents the load capacitance and is determined by factors such as fan-out, wire length, and transistor size. Vdd refers to the supply voltage, which decreases as the process nodes advance. In the context of the equation, the term α denotes the activity factor, which signifies the average frequency of wire and switch activity. On the other hand, f represents the clock frequency, which tends to rise as each successive process node is implemented. It's worth noting that the static power or leakage power is influenced by multiple factors,

including the supply voltage (V_{dd}), switching threshold (V_t), and transistor sizes.

V. CONCLUSIONS

leakage power has become a critical concern in VLSI design, demanding effective strategies for reduction at the system level. System-level power management techniques, such as dynamic voltage and frequency scaling, adaptive power management schemes, co-design methodologies, and power gating, offer promising avenues to mitigate leakage power. By considering the system as a whole and optimizing power consumption based on workload demands, temperature variations, and user requirements, designers can achieve significant improvements in energy efficiency and address the challenges posed by leakage power. The adoption of these system-level power management strategies not only reduces leakage power but also enhances overall performance, extends battery life, and contributes to the development of energy-efficient VLSI designs. Future research in this area should focus on exploring novel approaches and technologies to further advance leakage power reduction and meet the increasing demands for sustainable and power-efficient electronic systems.

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